AMENDMENTS TO THE CLAIMS

Please cancel claim 7 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to generate a data output signal in response to (i) a data input signal comprising a series of words, (ii) a valid word signal, and (iii) a select signal; and

a second circuit configured to generate said select signal in response to (i) said valid word signal, (ii) a start of frame signal, (iii) an end of frame signal and (iv) said data output signal, wherein (a) said select signal adjusts a starting point of each of said words to match a starting point of said first word and (b) said second circuit comprises (i) a decoder configured to present a length signal in response to said data output signal, (ii) a subtractor configured to present a sum signal in response to said length signal and a first enable signal and (iii) an adder circuit configured to generate said select signal in response to said sum signal.

2. (ORIGINAL) The apparatus according to claim 1, wherein said second circuit generates said select signal in further response to a clock signal.

3. (ORIGINAL) The apparatus according to claim 1, wherein said first circuit comprises a data circuit and said second circuit comprises a control circuit.

4. (ORIGINAL) The apparatus according to claim 1, wherein said first circuit comprises:

a first and a second register configured to arrange one or more bits of said data input signal; and

a multiplexer circuit configured to present said data output signal in response to said arranged bits.

5. (ORIGINAL) The apparatus according to claim 4, wherein said second register includes a data input configured to receive an output of said first register.

6. (ORIGINAL) The apparatus according to claim 4, wherein said first register and said second register are configured to receive said valid word signal.

7. (CANCELED)

8. (ORIGINAL) The apparatus according to claim 1, wherein said data input signal, said valid word signal, said start

of frame signal and said end of frame signal are received from a data source.

9. (CURRENTLY AMENDED) The apparatus according to claim 1 ~~7~~, wherein said second circuit further comprises a finite state machine configured to control said subtractor and said adder.

10. (ORIGINAL) The apparatus according to claim 9, wherein said second circuit further comprises:

a sum circuit configured to process said sum signal before said adder circuit generates said select signal.

11. (ORIGINAL) The apparatus according to claim 10, wherein said sum circuit presents an end message signal to said finite state machine.

12. (CURRENTLY AMENDED) A method for adjusting messages in hardware comprising:

(A) generating a data output signal in response to (i) a data input signal comprising a series of words, (ii) a valid word signal, and (iii) a select signal; and

(B) generating said select signal in response to (i) said valid word signal, (ii) a start of frame signal, (iii) an end of frame signal and (iv) said data output signal, wherein (a) said

select signal adjusts a starting point of each of said words to match a starting point of said first word and said method generates said select signal using (i) a decoder configured to present a length signal in response to said data output signal, (ii) a subtractor configured to present a sum signal in response to said length signal and a first enable signal and (iii) an adder circuit configured to generate said select signal in response to said sum signal.

13. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a data output signal in response to (i) a data input signal comprising a series of words, (ii) a valid word signal, and (iii) a select signal; and

means for generating said select signal in response to (i) said valid word signal, (ii) a start of frame signal, (iii) an end of frame signal and (iv) said data output signal, wherein (a) said select signal adjusts a starting point of each of said words to match a starting point of said first word and said apparatus generates said select signal using (i) a decoder configured to present a length signal in response to said data output signal, (ii) a subtractor configured to present a sum signal in response to said length signal and a first enable signal and (iii) an adder circuit configured to generate said select signal in response to said sum signal.